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Design of a Low-Power CMOS LVDS I/O Interface Circuit
circuit simulation with Samsung 0.18 m CMOS (complementary metal-oxide-semiconductor) standard technology under the 1.8 V supply voltage. Key words: Low-power circuit, LVDS, interface circuit, CMOS high-speed circuit, telescopic amplifier.
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CMOS offers high, symmetrical noise margins, high input and low output impedance, high packing density, and low power dissipation but speed is the only restricting factor. In contrast, the ECL gate has a high current drive per unit area, high switching speed, smaller propagation delay, but high power consumption makes very large scale integration difficult.

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This paper presents the design and implementation of a low power, highly linear, wideband RF front-end in 90 nm CMOS. The architecture consists of an inverter-like common gate low noise amplifier

Design and Analysis of Conventional P-FF using 90 nm CMOS ...

requirement in the low power digital circuit design. It has wide applications like low power CMOS design, Nano-technology, Digital signal processing. In this paper, I will design (modify) and analysis the Conditional Discharging Flip flop circuit, at the simulation TSMC 90nm technology for 1.8 V. Index Terms Flip flop, Conditional discharge, power consumption, Pulse triggered, 1. Pulse